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HP E2432A

Intel 80960CA/CF Preprocessor Interface

For use with HP logic analyzers

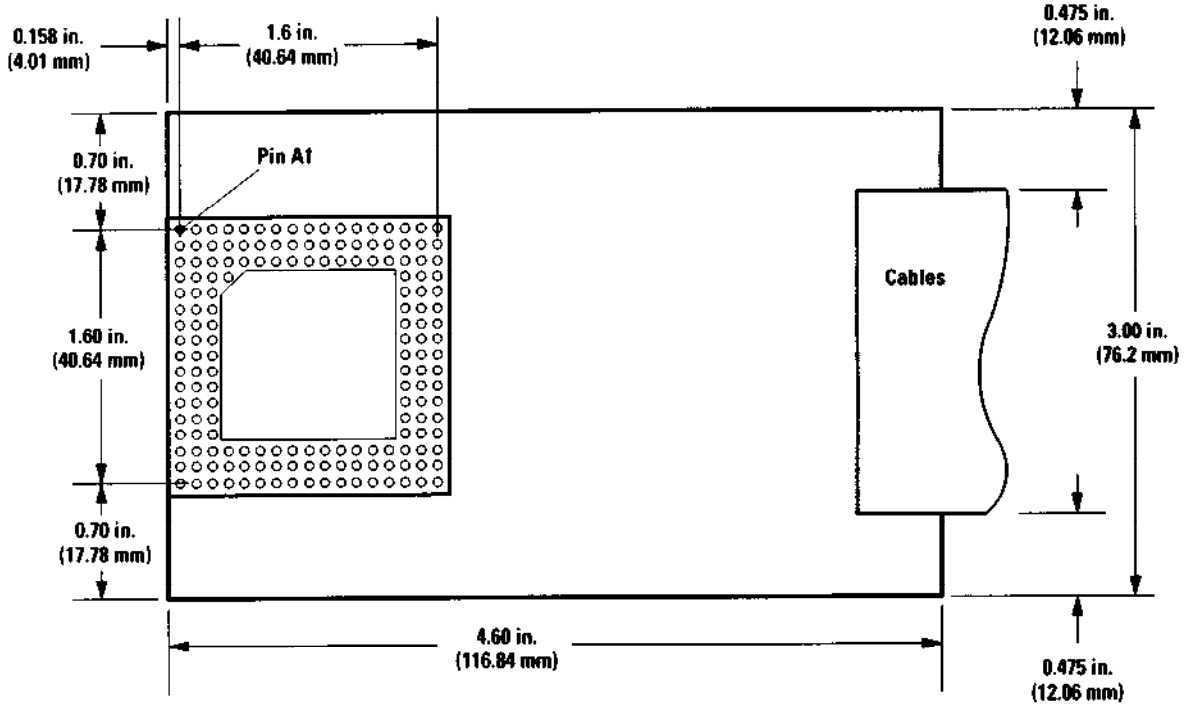
The HP E2432A preprocessor interface for the Intel 80960CA/CF is a mechanical and electrical interface between the Intel 80960CA/CF and various HP logic analyzers for real-time state analysis. The preprocessor routes signals; matches analyzer and chip setup and hold times; aligns address, data and status signals; and filters non-data transfers such as idle and wait states.

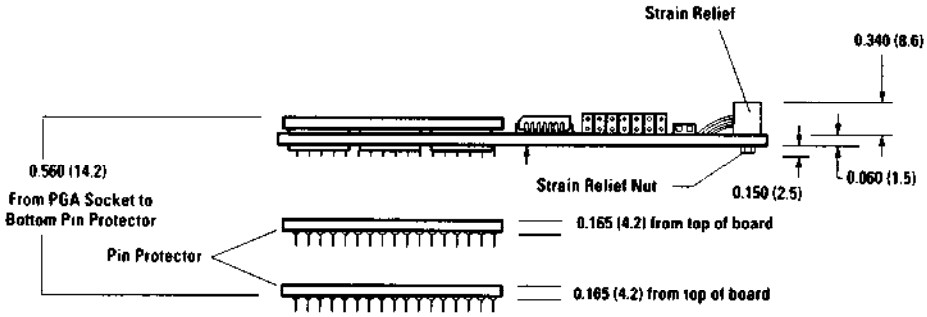
Preprocessor software configures the logic analyzer labeling address, data lines and status lines. Additionally, when a state trace is displayed, 80960 mnemonics are listed providing easy correlation between the data captured and the controlling program.

Microprocessor Supported:
Intel 80960CA/CF, 40-MHz, 168-pin PGA

Capabilities:

- The 80960CA/CF microprocessor can operate in a pipelined bus mode. The HP E2432A provides circuitry to align the address, data and status signals during pipelined bus cycles so the pipeline skew is transparent to the user.





- The HP E2432A filters states so that only valid data transfers (instruction fetches/ cache fills, data reads and writes) get clocked into the analyzer. Wait states, idle states (that is, states when the processor is not the bus master) do not get passed to the analyzer. This ensures optimal use of the analyzer's acquisition memory. One exception to this rule exists. The initial state of a HOLDA or BOFF# transaction is recorded so the user can see when the processor relinquishes control of the bus. Logic analyzer time tags can be used to measure the duration of these transactions.

- The 80960CA bus is configurable in 16 different memory regions. Six items can be configured within each region -- wait states, READY#/BTERM# enabling, bursting, pipelining, bus size and byte ordering. The HP E2432A supports each of these configurations. The 80960CF defines a seventh configuration item which is the ability to define a memory region that can be loaded into the microprocessor cache. The HP 2432A also supports this configuration.

- Monitors all 80960CA/CF signals of interest including the on-chip interrupt and DMA controllers.

Logic Analyzers supported:
HP 1650A/52A, HP 1650B/52B, HP 16510A/B, HP16511B, HP 16540/41[A-D], HP 16550A, HP1660A, HP 1661A.

Pods Required:
Five pods are required for inverse assembly. Two extra pods can be added to provide visibility of the on-chip interrrupt controller and DMA controller signals.

Termination Adapters (TAs):
Termination modules are provided for all seven pods. No additional TAs are required.

Signal Line Loading:
One 74F load on all signals except: One 74FCT load on PCLK1, PCLK2, A28, A29 and A30. DT/R#, CLKIN, and CLKMODE are left open (unloaded). All Vss lines are tied together and all Vcc and NC lines are left open.

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